WHAT IS CLAIMED IS:

1. A semiconductor memory device that performs read and write operations in synchronization with an external clock signal, comprising:

a frequency divider that divides the external clock signal by two and that generates a first clock signal for an even-numbered data patch and a second clock signal for an odd-numbered data, wherein the first clock signal is opposite in phase to the second clock signal;

a column selection line enable control circuit that generates even-numbered column selection line enable signals in response to the first clock signal and that generates odd-numbered column selection line enable signals in response to the second clock signal;

a switching circuit that connects a pair of bit lines to a pair of even-numbered input/output (I/O) lines in response to the even-numbered column selection line enable signals and that connects the pair of bit lines to a pair of odd-numbered I/O lines in response to the odd-numbered column selection line enable signals; and

an I/O line sense amplification circuit that senses and amplifies even-numbered read data from the pair of even-numbered I/O lines and outputs the amplified even-numbered read data to a pair of data lines in response to the first clock signal, and that senses and amplifies odd-numbered read data from the pair of odd-numbered I/O lines and outputs the odd-numbered read data to the pair of data lines in response to the second clock signal.

2. The semiconductor memory device of claim 1, further comprising a column address decoder that decodes an externally supplied column address and that provides the decoded column address to the column selection line enable control circuit.

3. The semiconductor memory device of claim 1, further comprising a write driver that receives even-numbered write data from the pair of data lines and provides the even-numbered write data to the pair of even-numbered I/O

lines in response to the first clock signal, and that receives odd-numbered write data from the pair of data lines and provides the odd-numbered write data to the pair of odd-numbered I/O lines in response to the second clock signal.

4. The semiconductor memory device of claim 1, further comprising a first precharge circuit that precharges the pair of even-numbered I/O lines in response to the first clock signal, and a second precharge circuit that precharges the pair of odd-numbered I/O lines in response to the second clock signal.